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Technology Scaling Impact on Embedded ADC Design for Telecom Receivers

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Abstract—This paper is concerned with the impact of technology scaling on the choice of A/D converters in telecom receivers. It is shown that the trend of diminishing feature size, together with better matching of passive components, allows the use of A/D topologies traditionally confined to low-frequency, medium-resolution applications. The design of a 10 bit 20 MS/s ADC using the successive approximation algorithm is presented in order to validate the presented concepts. By using a deep-submicron technology, the speed of the chosen architecture is pushed to meet the desired output rate.

I. INTRODUCTION

The prerequisite of Moore's law is the continued down-scaling of CMOS technology, which produces yet faster and more power-efficient digital circuitry. However, most technology parameters important for analog design suffer degradation in scaled technologies. As the minimum feature size decreases, so does the gate oxide thickness, causing still lower allowable supply voltages. The present state-of-the-art 90 nm technology node features a maximum supply voltage of only 1 V for the standard MOSTs. This supply is expected to decrease to 0.7 V for the future 45 nm node projected in 2010 [1]. As the device threshold voltages do not scale proportionally with decreasing supply voltage, the available voltage swing decreases which effectively disallows the use of stacked MOS circuit configurations. A common measure of technology speed is the device transition frequency f_T , given by [2]:

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gg} + C_{gb} + C_{gs} + C_{gd}} \quad (1)$$

where g_m is the transconductance. The capacitances C_{gg} , C_{gb} , C_{gs} and C_{gd} are the parasitic input, gate-bulk, gate-source and gate-drain capacitances respectively. As the minimum feature size decreases with each new technology node, the device g_m increases, whereas the parasitic capacitances decrease thus yielding ever-higher device f_T , which continues to increase the bandwidth of analog circuits. Furthermore, the availability of still better lithography processes, enhances the absolute matching of on-chip components for a fixed area [1].

Unfortunately, decreasing feature size also decreases the Early voltage V_A , which implies decreasing device output resistance r_o . Decreasing channel resistivity leads to decreasing intrinsic DC gain ($A_0 = g_m r_o$), thus reducing inherent circuit accuracy. Fig. 1 shows this trend for the recent technology scaling [2], [3], [4].

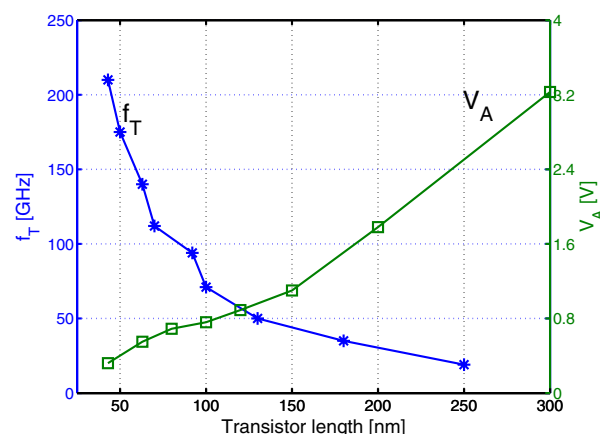


Fig. 1. Transistor f_T and early voltage vs. minimum length.

In the design of ADCs for telecom applications with a bandwidth in the MHz range, the increase of MOST response speed in scaled technologies allows the designer to consider topologies typically used only for low-frequency applications. However, reduced analog performance, especially in terms of gain, may be reflected in increased power consumption for a desired ADC accuracy as circuit complexity increases to compensate for intrinsic technology shortcomings. For this reason, a key feature of low-power ADCs in deep sub-micron technologies would be to use topologies that do not rely on high-gain feedback loops for successful operation. Further, the improved matching of passive devices in ever down-scaled technologies favors ADC topologies that are based on passive device matching.

II. THE CHOICE OF TELECOM RECEIVER ADCs

For many relevant telecom standards such as WLAN IEEE 802.11b and UMTS, typical ADC specifications for the receiver channel at base-band are in the range of 10 bits resolution at output rates of 20 MS/s, which can be achieved with different ADC topologies. Thus, the problem is to choose the best ADC topology for basically fixed specifications, while the technology-scaling trend continues. In addition, since portability in telecom applications is crucial, the main parameter for the ADC selection becomes power consumption minimization. This can be effectively achieved by using ADC architectures requiring more than one clock cycle per conversion (typically used only for low frequency applications) operated at very high frequency,

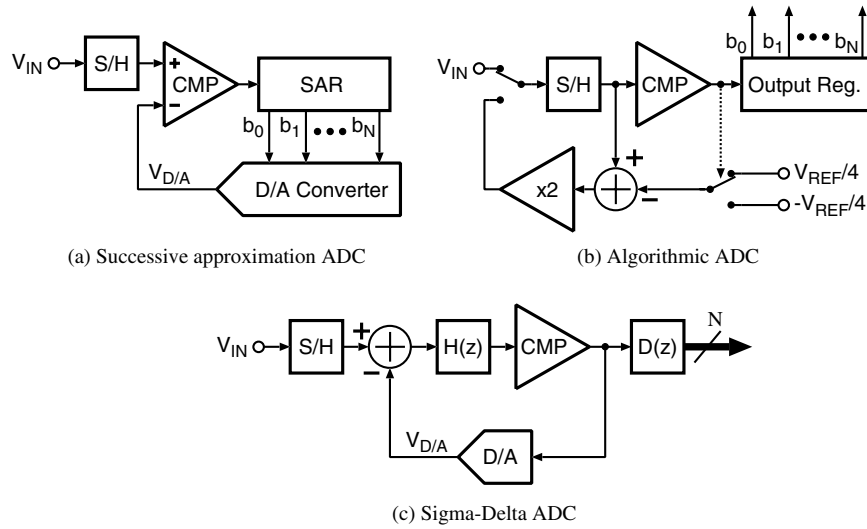


Fig. 2. ADC topologies utilizing a high degree of digital hardware for signal conversion.

exploiting the higher scaled-technology speed-of-response. The scaling also favors solutions where the majority of the necessary signal processing takes place in the digital domain and thus leaves us with a minimum of necessary analog hardware. Examples of such ADCs are $\Sigma\Delta$, algorithmic and successive approximation (SA) ADCs, shown conceptually in Fig. 2.

The key consideration in the selection among the above mentioned ADC architectures with respect to the technology scaling impact, is the effect of the voltage gain reduction. $\Sigma\Delta$ - and algorithmic ADCs process the input signal at each time slot of the conversion process, whereas the SA ADC only samples the reference during the conversion. In the following, the basic operation and the advantages/drawbacks of the before-mentioned architectures will be discussed.

A. $\Sigma\Delta$ -Modulator ADC

$\Sigma\Delta$ ADCs rely on shifting quantization noise out of the baseband by using analog filtering combined with oversampling and digital post-filtering for achieving the desired resolution. In each clock cycle, the quantization error is integrated by feeding the comparator output signal back to the modulator input. For a low-pass signal transfer function, the quantization noise transfer function (NTF) will be of high-pass type and the resulting double-sided inband quantization noise for a modulator of order N , can be approximated by:

$$\sigma_b^2 = \frac{\sigma_q^2}{f_s} \int_{-f_b}^{f_b} |NTF(f)|^2 df = \frac{\sigma_q^2}{f_s} \int_{-f_b}^{f_b} \left| \frac{f}{f_c} \right|^{2N} df, f_c \gg f_b \quad (2)$$

where σ_q^2/f_s is the quantization noise spread over the sampling frequency, f_b is the baseband frequency and f_c is the NTF cut-off frequency. For a finite integrator DC-gain A_0 , the NTF zeros will be shifted from DC to higher frequencies and thus allow more quantization noise to leak into the baseband. For a low-pass modulator of order N , the resulting excess noise factor can be shown to be [5]:

$$F=1+(2N+1) \left[\left(\frac{OSR}{2\alpha A_0} \right)^{2N} + \sum_{n=1}^{N-1} \frac{N(N-1) \dots N-n+1}{(2n+1)n!} \left(\frac{OSR}{2\alpha A_0} \right)^{2(N-n)} \right] \quad (3)$$

where $OSR = f_s/2f_b$ is the oversampling ratio and $\alpha = f_c/f_s$. From (3) it is seen that a high DC-gain is crucial for low excess noise performance. In [6], a full OTA is used for gain-boosting of all output stage cascodes in order to achieve the desired resolution of 14 bits at 25 MS/s in a $0.18 \mu\text{m}$ design, implying significant power increase for each integrator stage.

For downsampling to the desired output frequency, digital post-filtering and achieving the desired word-length, a decimator filter is needed as back-end for the $\Sigma\Delta$ ADC. Typically, the decimator is built from a number of filter stages of order $N+1$, each decimating by a factor of two and where the word-length increases for each decimation stage.

B. Algorithmic ADC

Whereas the $\Sigma\Delta$ ADC relies on frequency domain concepts for successful operation, the algorithmic ADC is best explained in the time-domain: the analog input signal is sampled in the beginning of the conversion phase. In each time-slot of the conversion phase, the sign of the present signal held is determined and the corresponding bit set. The present bit-value is used to feed back a signal of $\pm V_{ref}/4$ which is subtracted from the present held value. This residue signal is then multiplied by 2 and the next bit can be determined. Thus the same hardware is recycled in each time-slot of the conversion phase and at least $N+1$ clock cycles are needed for N bits overall ADC resolution.

The drawback is that a precise $\times 2$ block has to be implemented. For a resolution of N bits, a minimum DC-gain of $A_0 = 2^{N+1}$ is needed for precise residue forming, i.e. for keeping the initial error below $1/2$ LSB. This again requires a high-gain OTA to be implemented, even more so for ensuring a sufficient margin for a given desired resolution.

The desired settling has to be achieved within each time-slot of the conversion phase. Using a first order OTA model, the settling time constant τ , is given by:

$$\tau = \frac{1}{2\pi GBW} \quad (4)$$

where GBW is the OTA gain-bandwidth product. The minimum number n , of time-constants τ , for sufficient settling within a desired resolution is found from:

$$n > (N+1) \ln(2) \quad (5)$$

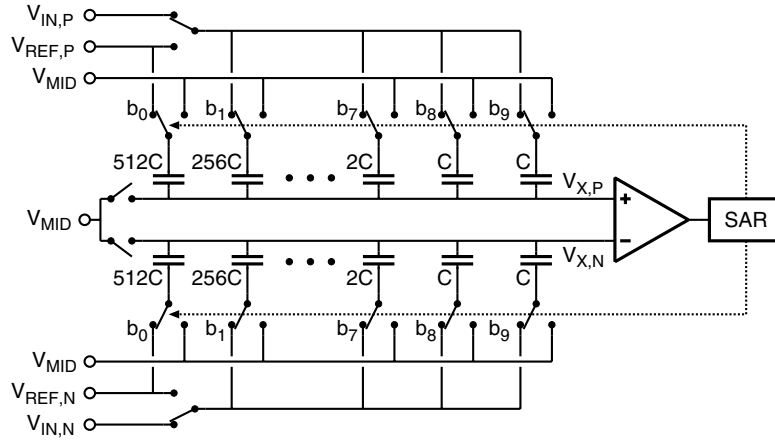


Fig. 3. Charge redistribution successive approximation ADC.

E.g. for an example resolution of 10 bits at 20 MS/s, a minimum gain of ≈ 66 dB would be needed and a GBW of ≈ 267 MHz for the residue OTA.

C. Successive Approximation (SA) ADC

The two previously presented ADC topologies require accurate analog signal processing functions to be realized employing still poorer gain stages if the maximum speed capability of the down-scaled technology is to be utilized, thus leading to higher power consumption in order to achieve the required performance. This is not the case for the SA ADC structure, which samples the input signal only at the beginning of the conversion cycle, and processes only the reference voltage during the time-slots in the conversion phase, using an open-loop topology.

As the signal is sampled, the successive approximation register (SAR) is reset to zero. Each bit in the output word is then tested by applying the present word value to the feedback DAC and comparing against the held input value. In other words, the SA ADC also requires a minimum of $N+1$ clock cycles for the entire conversion phase. The advantage over i.e. the algorithmic ADC is that no OTA is employed, but only a single open-loop comparator allowing for very high power efficiency and maximum analog hardware re-use as only a single comparator is needed. Furthermore, the input sample-and-hold block can be merged with the DAC using the charge redistribution structure first proposed in [7].

A drawback of the charge redistribution SA ADC is however that significant area is needed for the implementation of the sampling/DAC capacitors.

D. ADC topologies assessment

From the discussion, it is clear that the algorithmic ADC performance is determined by the accuracy of the residue amplifier, which in turn is directly related to the embedded OTA DC gain. Analogously, the $\Sigma\Delta$ ADC performance depends on the integrator performance, and consequently on the embedded OTA DC gain. On the contrary, the SA ADC can be implemented without any OTA using a capacitor array employed both for sampling the signal and for providing the feedback DAC signal. Thus, its performance does not depend on any OTA DC-gain, but rather on a single comparator used in open-loop configuration in each conversion step. The key advantage is that the behavior of open-loop comparators is

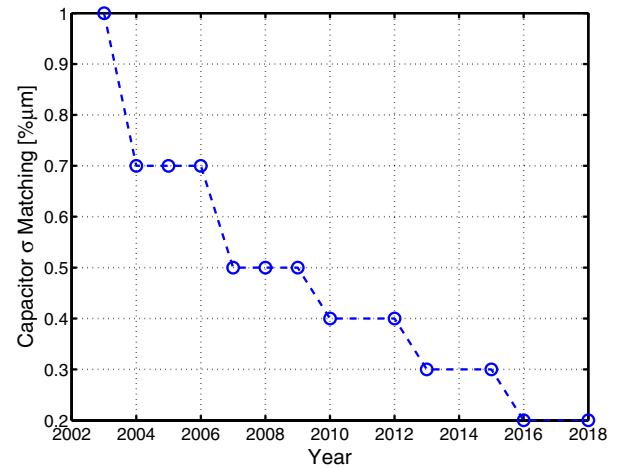


Fig. 4. Projected capacitor matching for future technologies.

much less affected by reduced DC gain, than that of closed-loop OTAs. As the same comparator is used for each cycle, potential offset will not affect the ADC performance. The achievable ADC output rate is then determined only by the achievable comparator speed.

Another drawback of the $\Sigma\Delta$ ADC topology, is that a decimator filter is needed which will consume significant area and power for large oversampling ratios and thus decrease the power efficiency of the ADC.

A common issue for all the presented ADC topologies is the implementation of efficient sampling switches under the low supply voltage constraint. This issue can largely be resolved by using the bootstrap technique for critical switches without significant power increase.

As a final consideration, two other reasons make the SA ADC choice preferable with future technologies. Firstly, the critical point of device mismatch sensitivity of SA ADCs becomes less important as the device matching improves in scaled technologies. This indicates that for achieving 10 bits accuracy, the mismatch robustness of $\Sigma\Delta$ topologies is no longer a pivotal feature. The projected matching for future technology nodes is shown in fig. 4 [1]. Secondly, the device f_T improvement, which is larger than the OTA gain-bandwidth product improvement in scaled technologies, leads to the choice of ADC topologies not relying on gain, but on high-speed blocks (like SA ADC).

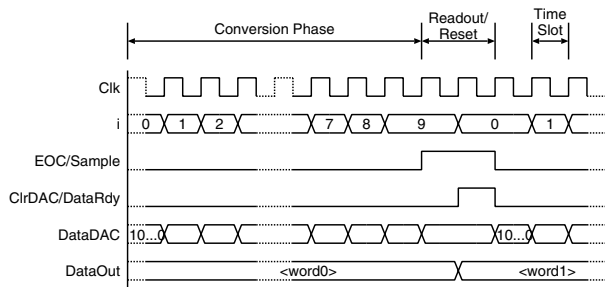


Fig. 5. ADC timing diagram.

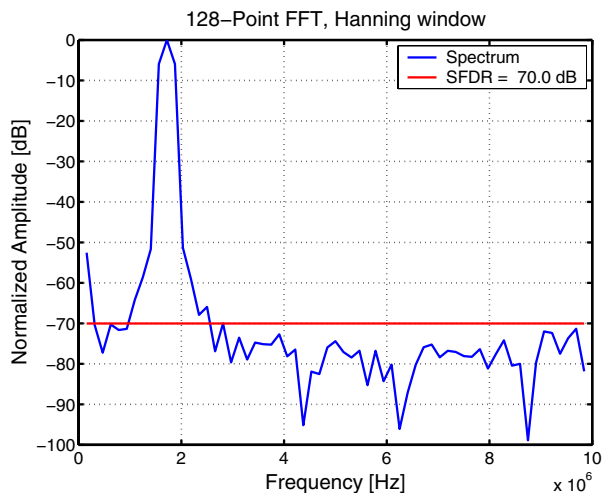


Fig. 6. ADC output spectrum.

III. TEST CIRCUIT

A. SA ADC topology

To demonstrate the above concept, a 10 bit 20 MS/s SA ADC prototype is proposed, using the capacitor charge redistribution topology. The circuit has been designed in a 1P6M 0.13 μm CMOS process and is currently being fabricated. A block diagram schematic of the implemented circuit is shown in fig. 3. The capacitors are implemented as arrays of 50 fF unit MIM capacitors. The ADC needs 12 clock cycles for each conversion phase, where 10 cycles are used for the actual conversion and 2 cycles for readout and reset of the ADC. The extra clock cycle allows for using two cycles for input signal sampling as precise acquisition is crucial for succesful conversion. The timing diagram is shown in fig. 5.

B. Simulation results

An example output spectrum from a full transistor level simulation including all digital blocks, applying a 1.72 MHz input tone at a 20 MS/s output rate and a 240 MHz input clock, is given in Fig. 6. The ADC performance alongside with key parameters is summarized in table I. In Fig. 7, a comparison with state-of-the-art ADCs, using a figure-of-merit $\text{FoM} = P/(2^N f_{\text{out}})$, is shown. As seen, the proposed design is highly competitive with current state-of-the-art, demonstrating the validity of the above considerations.

IV. CONCLUSION

In this paper, the impact of technology scaling on the choice of ADC topology suitable for telecom receivers has been discussed. It is found that the speed improvement in deep submi-

TABLE I
PERFORMANCE SUMMARY.

Supply voltage	1.2 V
Power consumption (incl. buffers)	4 mW
Input voltage peak-peak	900 mV
SFDR(@ $f_{\text{tone}} = 1.72 \text{ MHz}$)	> 70 dB
Technology	1P6M 0.13 μm CMOS
Active area	0.75 mm^2
Conversion rate	20 MS/s
Input clock rate	240 MHz

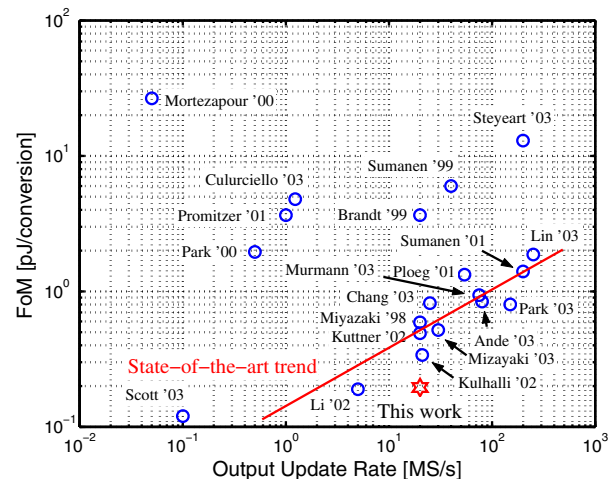


Fig. 7. Figure-of-Merit Comparison.

cron technologies enables the use of power-efficient, hardware recycling type ADCs traditionally employed for low-frequency applications. Of the three particular topologies investigated; $\Sigma\Delta$, algorithmic and SA ADC, the SA ADC is found to be best suited for future technologies as it does not rely on difficult-to-implement high-gain feedback components but rather utilizes the improved speed and passive component matching inherent to deep submicron processes. A test design of a 10 bit 20 MS/s SA ADC in a 0.13 μm CMOS process is presented and the simulation results indicate that our target specifications are indeed reachable. Due to the high power efficiency of the circuit, a highly competitive FoM results, validating the considerations for power-efficient ADC design in modern technologies as presented in this paper.

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